What is claimed is:

1. A method of operating a non-volatile memory device comprising:

coupling a precharge voltage on a substrate tub of a NAND architecture memory array of a plurality of floating gate memory cells, wherein the plurality of floating gate memory cells are coupled in a plurality of strings;

coupling a gate programming voltage to the gate of a selected floating gate memory cell of each string of a selected number of strings; and

selectively coupling a program voltage or a program-inhibit voltage to a channel of each string of the selected number of strings.

2. The method of claim 1, wherein the non-volatile memory device is one of a Flash memory device and a EEPROM memory device.

3. The method of claim 1, wherein the gate programming voltage is approximately 20V.

4. The method of claim 1, wherein the precharge voltage is approximately 5V.

5. The method of claim 1, wherein the program voltage is approximately ground and the program-inhibit is approximately Vcc.

6. The method of claim 1, further comprising:

coupling a pass voltage to the gates of one or more non-selected floating gate memory cells of each string of the selected number of strings.

7. The method of claim 6, wherein the pass voltage level is approximately 10V.

8. The method of claim 1, wherein coupling the precharge voltage on the substrate tub and coupling the gate programming voltage to the gate of the selected floating gate

memory cell of each string of the selected number of strings, further comprises coupling the precharge voltage on the substrate tub and coupling the gate programming voltage to the gate of the selected floating gate memory cell of each string of the selected number of strings after uncoupling the precharge voltage.

9. The method of claim 1, wherein coupling the precharge voltage on the substrate tub and coupling the gate programming voltage to the gate of the selected floating gate memory cell of each string of the selected number of strings, further comprises coupling the precharge voltage on the substrate tub and coupling the gate programming voltage to the gate of the selected floating gate memory cell of each string of the selected number of strings before uncoupling the precharge voltage.

10. The method of claim 1, wherein coupling the precharge voltage on the substrate tub and coupling the gate programming voltage to the gate of the selected floating gate memory cell of each string of the selected number of strings, further comprises coupling the precharge voltage on the substrate tub and coupling the gate programming voltage to the gate of the selected floating gate memory cell of each string of the selected number of strings and uncoupling the precharge voltage after the gate programming voltage has reached a selected voltage level.

11. The method of claim 10, wherein the selected voltage level is a gate programming voltage level of approximately 5V.

12. The method of claim 1, wherein selectively coupling a program voltage or a program-inhibit voltage to a channel of each string of the selected number of strings further comprises selectively coupling a program voltage or a program-inhibit voltage to a channel of each string of the selected number of strings through a drain select gate transistor.

13. The method of claim 1, wherein selectively coupling a program voltage or a

program-inhibit voltage to a channel of each string of the selected number of strings further comprises selectively coupling a program voltage or a program-inhibit voltage to a channel of each string of the selected number of strings when the gate programming voltage is coupled to the gate of the selected floating gate memory cell of each string of the selected number of strings.

14. The method of claim 1, wherein selectively coupling a program voltage or a program-inhibit voltage to a channel of each string of the selected number of strings further comprises selectively coupling a program voltage or a program-inhibit voltage to a drain of a first floating gate memory cell of each string of the selected number of strings.

15. The method of claim 1, wherein small feature low voltage circuit elements are used in a coupled bitline circuit and a coupled source line circuit.

16. The method of claim 15, wherein the coupled bitline circuit has a decoder or a multiplexer.

17. A method of operating a non-volatile memory device comprising:

generating a channel of carriers in a selected plurality of floating gate memory cells of a memory array, where the memory cells are coupled in a plurality of strings by:

placing a precharge voltage on a substrate tub that is coupled to the memory array; and

programming a selected floating gate memory cell of a selected number of strings by:

removing the precharge voltage from the substrate tub,

placing a gate programming voltage on the control gate of the selected floating gate memory cell of the selected number of strings, and

selectively placing a program voltage or a program-inhibit voltage on a

bitline coupled to a a channel of each string of the selected number of strings.

18. The method of claim 17, wherein the non-volatile memory device is one of a Flash memory device and a EEPROM memory device.

19. The method of claim 17, further comprising:
placing a plurality of word lines coupled to a plurality of control gates of the selected plurality of memory cells in a high impedance state.

20. The method of claim 17, further comprising:
placing a plurality of bitlines coupled to the plurality of strings in a high impedance state.

21. The method of claim 17, further comprising:
placing at least one source line coupled to the plurality of strings in a high impedance state.

22. The method of claim 17, further comprising:
placing approximately 4.5V on at least one source line coupled to the plurality of strings.

23. The method of claim 22, wherein placing approximately 4.5V on at least one source line coupled to the plurality of strings further comprises placing 4.5V on at least one source line coupled to the plurality of strings through a plurality of source line gate transistors coupled to a source of a final floating gate memory cell of each string of the plurality of strings.

24. The method of claim 17, further comprising:
placing approximately Vcc on at least one source line coupled to the plurality of

strings.

25. The method of claim 24, wherein Vcc is one of 3.3V and 1.8V.

26. The method of claim 17, wherein programming a selected floating gate memory cell of a selected number of strings, further comprises:
placing a pass voltage on the non-selected floating gate memory cells of the selected number of strings.

27. The method of claim 26, wherein placing a pass voltage on the non-selected floating gate memory cells further comprises placing an approximately 10V pass voltage on the non-selected floating gate memory cells.

28. The method of claim 17, wherein programming a selected floating gate memory cell of a selected number of strings by placing a gate programming voltage on the control gate of the selected floating gate memory cell further comprises programming a selected floating gate memory cell of a selected number of strings by placing an approximately 20V gate programming voltage on the control gate of the selected floating gate memory cell.

29. The method of claim 17, wherein generating a channel of carriers in a selected plurality of floating gate memory cells by placing a precharge voltage on a substrate tub further comprises generating a channel of carriers in a selected plurality of floating gate memory cells by placing an approximately 5V precharge voltage on a substrate tub.

30. The method of claim 17, wherein programming a selected floating gate memory cell of a selected number of strings by removing the precharge voltage from the substrate tub further comprises removing the precharge voltage and bringing the substrate tub to a selected normal substrate tub volatge.

31. The method of claim 17, wherein programming a selected floating gate memory cell of a selected number of strings by removing the precharge voltage from the substrate tub further comprises removing the precharge voltage and grounding the substrate tub.

32. The method of claim 17, wherein programming a selected floating gate memory cell of a selected number of strings by removing the precharge voltage from the substrate tub further comprises removing the precharge voltage from the substrate tub after placing the gate programming voltage on the control gate of the selected floating gate cell.

33. The method of claim 32, wherein removing the precharge voltage from the substrate tub after placing the gate programming voltage on the control gate of the selected floating gate cell further comprises removing the precharge voltage from the substrate tub after the gate programming voltage reaches a selected voltage level.

34. The method of claim 33, wherein the selected voltage level of the gate programming voltage is approximately 5V.

35. The method of claim 17, wherein programming a selected floating gate memory cell of a selected number of strings by removing the precharge voltage from the substrate tub further comprises removing the precharge voltage from the substrate tub before placing the gate programming voltage on the control gate of the selected floating gate cell.

36. The method of claim 17, wherein an erase circuit coupled to the substrate tub generates the precharge voltage.

37. The method of claim 17, wherein low voltage circuit elements are used in a coupled bitline circuit and a coupled source line circuit.

38. A method of programming a NAND architecture floating gate memory cell string comprising:

precharging a channel of carriers in the NAND architecture floating gate memory cell string;

coupling a gate programming voltage to the gate of a selected floating gate memory cell of the string;

coupling a high pass voltage to the gates one or more non-selected floating gate memory cells of the string; and

selectively coupling a program voltage or a program-inhibit voltage to a channel of the string.

39. The method of claim 38, wherein precharging a channel of carriers in the NAND architecture floating gate memory cell string further comprises precharging a channel of carriers in the NAND architecture floating gate memory cell string by coupling a precharge voltage to from a substrate tub.

40. The method of claim 38, wherein precharging a channel of carriers in the NAND architecture floating gate memory cell string and coupling a gate programming voltage to the gate of a selected floating gate memory cell of the string, further comprises precharging a channel of carriers in the NAND architecture floating gate memory cell string and coupling a gate programming voltage to the gate of a selected floating gate memory cell of the string after uncoupling the precharge voltage.

41. The method of claim 38, wherein precharging a channel of carriers in the NAND architecture floating gate memory cell string and coupling a gate programming voltage to the gate of a selected floating gate memory cell of the string, further

comprises precharging a channel of carriers in the NAND architecture floating gate memory cell string and coupling a gate programming voltage to the gate of a selected floating gate memory cell of the string before uncoupling the precharge voltage.

42. The method of claim 38, precharging a channel of carriers in the NAND architecture floating gate memory cell string and coupling a gate programming voltage to the gate of a selected floating gate memory cell of the string, further comprises precharging a channel of carriers in the NAND architecture floating gate memory cell string and coupling a gate programming voltage to the gate of a selected floating gate memory cell of the string and uncoupling the precharge voltage after the gate programming voltage has reached a selected voltage level.

43. The method of claim 38, wherein selectively coupling a program voltage or a program-inhibit voltage to a channel of the string, further comprises selectively coupling a program voltage or a program-inhibit voltage to a channel of the string when the gate programming voltage is coupled to the gate of the selected floating gate memory cell of the string.

44. A method of programming a NAND architecture floating gate memory cell array comprising:

applying a precharge voltage to a substrate tub of the NAND architecture memory array, wherein the NAND architecture memory array contains a plurality of floating gate memory cells serially coupled source to drain in a plurality of strings;

applying a programming voltage to a selected floating gate memory cell of each string of a selected number of strings;

applying a pass voltage to one or more non-selected floating gate memory cells of each string of the selected number of strings; and

selectively applying a program voltage to a drain of a channel of each string of the

selected number of strings.

45. The method of claim 44, wherein selectively applying a program voltage to a drain of a channel of each string of the selected number of strings, further comprises selectively applying a program voltage or a program-inhibit voltage to a drain of a channel of each string of the selected number of strings.

46. A method of programming a floating gate transistor memory cell comprising:
generating a channel of carriers in the floating gate transistor memory cell by coupling a precharge voltage on a substrate tub the floating gate transistor memory cell is formed on;
coupling a gate programming voltage to the floating gate transistor memory cell of each string of a selected number of strings; and
coupling a program voltage or a program-inhibit voltage to the channel of the floating gate transistor memory cell.

47. The method of claim 46, wherein the floating gate transistor is coupled in series to at least one additional floating gate memory cell.

48. A memory device comprising:
a substrate tub;
a floating gate memory cell in series with at least one additional floating gate memory cell formed in the substrate tub;
a word line coupled to a gate of the floating gate memory cell;
a bitline coupled to a drain of the floating gate memory cell; and
a source line coupled to a source of the floating gate memory cell, wherein the memory device is adapted to precharge a channel in the floating gate memory cell with a precharge voltage on the substrate tub and program the floating gate memory cell with a floating gate programming voltage on the gate and a program voltage or a program-inhibit voltage that is selectively

coupled to the drain.

49. The memory device of claim 48, wherein the floating gate memory cell is one of a plurality of floating gate memory cells arranged in a memory array, where the plurality of memory cells are coupled into a plurality of strings of memory cells with the floating gate memory cells in each string serially coupled source to drain, where a drain of a first floating gate memory cell of each string is coupled to the bitline and a source of a final floating gate memory cell of each string is coupled to the source line.

50. The memory device of claim 49, wherein the drain of the first floating gate memory cell of each string of floating gate memory cells is coupled to a drain select gate transistor and the source of the final floating gate memory cell is coupled to a source select gate transistor.

51. The memory device of claim 49, wherein the memory device is adapted to precharge a channel in a selected string of the floating gate memory cells with the precharge voltage on the substrate tub and to program a selected floating gate memory cell of the string with the gate programming voltage on the gate of the selected floating gate memory cell and a program voltage or a program-inhibit voltage that is selectively coupled to the drain of the first floating gate memory cell of the selected string.

52. The memory device of claim 49, wherein the memory device is adapted to couple a pass voltage to the unselected floating gate memory cells of a selected string of floating gate memory cells.

53. The memory device of claim 48, wherein the memory device is adapted to remove the precharge voltage of the substrate tub before programming the floating gate memory cell by asserting the gate programming voltage on the gate and the

program voltage or the program-inhibit voltage to the drain.

54. The memory device of claim 48, wherein the memory device is adapted to remove the precharge voltage of the substrate tub after asserting the gate programming voltage on the gate and the program voltage or the program-inhibit voltage to the drain to program the floating gate memory cell.

55. The memory device of claim 54, wherein the memory device is adapted to remove the precharge voltage of the substrate tub after the gate programming voltage has been asserted on the gate and reached a selected voltage level.

56. The memory device of claim 48, wherein the memory device is a non-volatile memory device.

57. A Flash memory device comprising:

a NAND architecture memory array formed on at least one substrate tub having a plurality of floating gate memory cells arranged in rows and columns and coupled into a plurality of strings;

a plurality of word lines, wherein each word line is coupled to one or more gates of a row of the floating gate memory cells;

a plurality of bitlines, wherein each bitline is coupled to a drain of a first floating gate memory cell of one or more strings;

at least one source line, wherein the at least one source line is coupled to a source of a last floating gate memory cell of one or more strings;

wherein the Flash memory device is adapted to couple a precharge voltage on the at least one substrate tub to precharge a channel in the plurality of strings of floating gate memory cells; and

wherein the Flash memory device is adapted to program a selected floating gate memory cell of each of a selected number of strings of floating gate memory cells by applying a gate programming voltage to the gate of the

selected floating gate memory cell through the coupled word line and by applying a selected program voltage or a program-inhibit voltage through the coupled bitline.

58. The Flash memory device of claim 57, wherein the Flash memory device is adapted to remove the coupled precharge voltage of the substrate tub before programming the selected floating gate memory cell of each of a selected number of strings of floating gate memory cells by applying a gate programming voltage to the gate of the selected floating gate memory cell through the coupled word line and by applying a selected program voltage or a program-inhibit voltage through the coupled bitline.

59. The Flash memory device of claim 57, wherein the Flash memory device is adapted to remove the coupled precharge voltage of the substrate tub after applying the gate programming voltage to the gate of the selected floating gate memory cell.

60. The Flash memory device of claim 59, wherein the Flash memory device is adapted to remove the precharge voltage of the substrate tub after the gate programming voltage has been applied to the gate of the selected floating gate memory cell and has reached a predetermined voltage level.

61. The Flash memory device of claim 57, wherein the Flash memory device is adapted to selectively adjust the precharge voltage of the substrate tub.

62. The Flash memory device of claim 57, wherein the Flash memory device is adapted to selectively adjust the precharge voltage of the substrate tub to alter programming disturb characteristics of the floating gate memory cells of the array.

63. The Flash memory device of claim 57, wherein the substrate tub is a P doped well area.

64. The Flash memory device of claim 57, wherein the substrate tub is a silicon on insulator (SOI) area.

65. The Flash memory device of claim 57, wherein the Flash memory device is adapted to place the plurality of word lines in a high impedance state while the precharge voltage is applied to the substrate tub.

66. The Flash memory device of claim 57, wherein the Flash memory device is adapted to drive the plurality of word lines with a selected voltage while the precharge voltage is applied to the substrate tub.

67. The Flash memory device of claim 57, wherein the Flash memory device is adapted to place the plurality of bitlines in a high impedance state while the precharge voltage is applied to the substrate tub.

68. The Flash memory device of claim 57, wherein the Flash memory device is adapted to drive the plurality of bitlines with a selected voltage while the precharge voltage is applied to the substrate tub.

69. The Flash memory device of claim 57, wherein the Flash memory device is adapted to place the one or more source lines in a high impedance state while the precharge voltage is applied to the substrate tub.

70. The Flash memory device of claim 57, wherein the Flash memory device is adapted to drive the one or more source lines with a selected voltage while the precharge voltage is applied to the substrate tub.

71. A NAND architecture floating gate memory cell string comprising:
a NAND architecture floating gate memory cell memory string formed on a

substrate tub having a plurality of floating gate memory cells coupled source to drain in a serial string;

wherein the substrate tub is adapted to apply a precharge voltage to precharge carriers in a channel of the floating gate memory cells of the string; and

wherein the NAND architecture floating gate memory cell memory string is adapted to program a selected floating gate memory cell of the string by placing a gate programming voltage on the gate of the selected floating gate memory cell and a program voltage or a program-inhibit coupled to the channel of floating gate memory cell memory string.

72. The NAND architecture floating gate memory cell string of claim 71, further comprising:

a plurality of word lines, wherein each word line is coupled to a gate of a floating gate memory cell of the string;

a plurality of bitlines, wherein each bitline is coupled to a drain of a first floating gate memory cell of the string; and

at least one source line, wherein the at least one source line is coupled to a source of a last memory cell of the string.

73. The NAND architecture floating gate memory cell string of claim 71, wherein the NAND architecture floating gate memory cell memory string is adapted to couple a program-inhibit voltage to the channel of floating gate memory cell memory string.

74. The NAND architecture floating gate memory cell string of claim 71, wherein the floating gate memory cells are NMOS floating gate transistors.

75. The NAND architecture floating gate memory cell string of claim 71, wherein the floating gate memory cells are PMOS floating gate transistors.

76. The NAND architecture floating gate memory cell string of claim 71, wherein the

NAND architecture floating gate memory cell memory string is adapted to actively discharge the substrate tub after removing the applied precharge voltage.

77. A NAND architecture Flash memory device comprising:

a NAND architecture memory array formed on a substrate tub having a plurality of floating gate memory cells arranged in rows and columns in a plurality of erase blocks, wherein the plurality of floating gate memory cells are serially coupled source to drain into a plurality of serial strings;

a control circuit;

a row decoder coupled to a plurality of word lines, wherein each word line is coupled to one or more gates of a row of the floating gate memory cells;

a plurality of bitlines, wherein each bitline is coupled to a first floating gate memory cell of one or more strings through a drain control gate transistor;

at least one source line, wherein the at least one source line is coupled to a last memory cell of one or more strings through a source control gate transistor;

wherein the control circuit is adapted to couple a precharge voltage to the substrate tub to precharge a channel of carriers in the plurality of strings of floating gate memory cells; and

wherein NAND architecture Flash memory device is adapted to program a selected floating gate memory cell of each of a selected number of strings of floating gate memory cells by placing a gate programming voltage on the gate of the selected floating gate memory cell through the coupled word line and by placing a selected program voltage or a program-inhibit voltage on the coupled bitline while a high pass voltage is placed on the gates of the non-selected floating gate memory cells.

78. The NAND architecture floating gate memory device of claim 77, wherein the NAND architecture Flash memory device is adapted to turn on the drain control gate transistor during programming the selected floating gate memory cell and couples the selected program voltage or program-inhibit voltage that is placed on

the coupled bitline.

79. The NAND architecture floating gate memory device of claim 77, wherein the NAND architecture Flash memory device is adapted to turn on the source control gate transistor when the precharge and programming voltages are applied to the selected number of strings.

80. The NAND architecture floating gate memory device of claim 77, wherein the NAND architecture Flash memory device is adapted to turn off the source control gate transistor when the precharge and programming voltages are applied to the selected number of strings.

81. A system comprising:

a host coupled to a Flash memory device, wherein the Flash memory device comprises,

a NAND architecture memory array formed on at least one substrate tub having a plurality of floating gate memory cells arranged in rows and columns and coupled into a plurality of strings;

a plurality of word lines, wherein each word line is coupled to one or more gates of a row of the floating gate memory cells;

a plurality of bitlines, wherein each bitline is coupled to a drain of a first floating gate memory cell of one or more strings;

at least one source line, wherein the at least one source line is coupled to a source of a last floating gate memory cell of one or more strings;

wherein the Flash memory device is adapted to couple a precharge voltage on the at least one substrate tub to precharge a channel in the plurality of strings of floating gate memory cells; and

wherein the Flash memory device is adapted to program a selected floating gate memory cell of each of a selected number of strings of floating gate memory cells by applying a gate programming voltage to the

gate of the selected floating gate memory cell through the coupled word line and by applying a selected program voltage or a program-inhibit voltage through the coupled bitline.

82. The system of claim 81, wherein the host is a processor.

83. The system of claim 81, wherein the host is a computer system.

84. A Flash memory device comprising:

a NAND architecture memory array formed on a substrate tub having a plurality of floating gate memory cells arranged in rows and columns and coupled into a plurality of strings;

a plurality of word lines, wherein each word line is coupled to one or more gates of a row of the floating gate memory cells;

a plurality of bitlines, wherein each bitline is coupled to a drain of a first floating gate memory cell of one or more strings;

at least one source line, wherein the at least one source line is coupled to a source of a last floating gate memory cell of one or more strings;

a means for applying a precharge voltage on the substrate tub;

a means for programming a selected floating gate memory cell of each of a selected number of strings of floating gate memory cells; and

a means for program-inhibiting a selected floating gate memory cell of each of a selected number of strings of floating gate memory cells.